REMARKS

Claim Rejections Under 35 USC 103(a)

Claims 25-39 have been rejected under 35 USC 103(a) as being unpatentable over Hembree (US Patent No. 5,783,461) in view of Pedder (US Patent No. 5,717,245). In response to the 35 USC §103 rejections, claims 25-39 have been amended, and claims 47-53 have been added. In addition, the Examiner is asked to consider the arguments to follow. Also non-elected claims 40-46 have been canceled, and the specification has been amended to include patent number for the cited applications.

Summary of the Invention

The claims are directed to a "semiconductor component". In the elected embodiment of Figures 1-7, the component can comprise a chip module 24 (Figure 2E), a multi chip module 28 (Figure 3) or a semiconductor package 72 (Figure 7). In each case, the component includes a substrate 10 (Figure 2) and a blanket deposited conductive layer 14 (Figure 2) on the substrate 10. In addition, the component includes conductors 16 (Figure 2) on the substrate 10, and a semiconductor die 20 (Figure 2E, 3A or 7) in electrical communication with the conductors 16. The die 20 can be "flip chip" mounted as shown in Figure 2E, or "wire bonded" as shown in Figure 3A.

Each conductor 16 is defined by a pair of laser machined grooves 15 (Figure 2) in the conductive layer 14. As shown in Figure 2C, the conductors 16 comprise portions of the conductive layer 15 are also separated by remaining portions of the conductive layer 15. In addition, as shown in Figure 2, each conductor 16 includes bond pads 18 (contacts) configured for flip chip mounting or wire bonding the die 20, and can also include contact pads 22 (contacts) configured for electrical connection to outside circuitry. In the case of wire bonding, an opening 40 (Figure 3A) can be laser machined in the conductive layer 14 for attaching the die 20 to the substrate. As shown in Figure 5A, the substrate 10BGA

can also include conductive vias 58 in electrical communication with the conductors 16BGA, and contact balls 66 in electrical communication with the conductive vias 58.

Argument

MPEP 2142, 2143 set forth the three basic criteria for establishing a prima facie case of obviousness under 35 USC §103(a). First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success in obtaining the claimed invention based upon the references relied upon by the Examiner. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicants would first argue that the amended claims include limitations that are not suggested by the cited combination of references. One non-suggested limitation in each independent claim is that the "conductors" are stated to be "defined by a plurality of laser machined grooves", and to comprise "portions of the conductive layer electrically isolated from one another by the grooves". In addition, in independent claim 25 the conductors are stated to be "separated from one another by remaining portions of the conductive layer" (antecedent basis on page 8, lines 13-15 of the specification).

With the presently claimed conductors, and as shown in Figure 2, the bulk of the conductive layer 14 remains to protect the substrate 10, and only the conductive layer in the laser machined grooves 15 is removed. As the laser machined grooves 15 can be made extremely small and closely spaced, the conductors 16 can also be small and closely spaced.

This conductor construction is different than conventional etched or deposited conductors. For example, in

Hembree et al., the base 14 of the temporary semiconductor package 10 includes conductors 40 (Figure 1), and the interconnect 16 on the base 14 include conductors 58 (Figure 4). However, the conductors 40 are formed using conventional metallization processes (column 5, lines 64-67 and column 6, lines 16-20). Similarly, the conductors 58 (Figure 4) on the interconnect 16 are formed using an etching or deposition process (See US Patent Nos. 5,326,428 and 5,419,807 cited at column 6, lines 50-54). In either case, there are no laser machined grooves, and no portions of a conductive layer (other than the conductors 40 or 58) remains on the base 14 or the interconnect 16.

Pedder teaches a semiconductor package 10 having a substrate 12 which comprises separate metallization layers 30, 31, 32 (Figure 3). As stated at column 4, lines 11-18 of Pedder a metallization pattern (microstrips) are formed using a "screen printing process". With such a process, there is no remaining conductive layer on the substrate as presently claimed.

Further, the microstrips in Pedder have a different structure than the present conductors. As stated at column 6, line 63 to column 7, line 4, of Pedder:

"In order to achieve tighter tolerances, a combination of triplate and surface microstrip constructions are employed to allow trimming and tuning of these components after manufacture. This is realized by arranging for the majority of the length of a resonator or filter element to be defined in the triplate format described above, but completing the length with the addition of a short length of microstrip formed in the upper or lower metallisation. This measure takes part of the element onto the package surface, where laser or abrasive trimming may be employed to adjust the length and resonant behavior of the line."

However, with the Pedder laser trimming process, there would be no laser machined grooves in a conductive layer which define the microstrips (conductors) as presently claimed. Rather, only the length of the microstrips (conductors) is laser trimmed, and the width is conventional.

The laser machined microstrips in Pedder thus have a different structure than the conductors presently claimed.

Independent claim 35 also recites the limitation of "the thickness of the conductive layer, and a width of the conductors selected to provide a selected impedance for the conductors." Although impedance adjustment is known in the art, conductors having an impedance adjusted by laser machined grooves in a conductive layer are submitted to be unobvious over the art.

Independent claim 47 also recites the feature of the conductors including "first contacts on first ends thereof configured for bonding" (bond pads 18-Figure 2), and "second contacts on second ends thereof configured for electrical connection to external circuitry" (contact pads 22-Figure 2). Independent claim 52 recites "contacts" (bond pads 18-Figure 2) in combination with "conductive vias". It is submitted that conductors and contacts in combination, which comprise laser machined grooves in a conductive layer, are unobvious over the art.

Dependent claims 31 and 51 also recite the feature of a laser machined opening in the conductive layer for mounting the die (opening 40-Figure 3A). It is submitted that a component having a laser machined opening, and laser machined conductors in combination, is unobvious over the art.

Applicants would further argue that one skilled in the art would have no incentive to combine Hembree et al. and Pedder in the manner of the Office Action. In Pedder laser machining is used to trim the length of microstrips in order to adjust the electrical resonant frequency and bandpass characteristics of "resonator or filter elements" (column 6, lines 58-60). As resonator or filter elements are not used in Hembree et al., there would be no reason to precisely trim the lengths of the conductors by laser machining.

Conclusion

In view of the above amendments and arguments, favorable consideration and allowance of amended claims 25-39 and added claims 47-53 is requested. Should any issues remain, the Examiner is asked to contact the undersigned by telephone.

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April 9, 2001
Date of Signature

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Marked Version Of Amended Specification

On page 17, line 17, after "08/993,965" add --, now U.S. Patent No. 6,107,109,--.

On page 16,, line 8, after "08/726,349" add --, now U.S. Patent No. 5,783,461,--.

Marked Version Of Amended Claims

25. (amended) A semiconductor component comprising;

a substrate [comprising] having a first surface and an opposing second surface;

[with a conductive layer thereon, and a second surface;]

a conductive layer on the first surface;

a plurality of conductors on the first surface [, each conductor comprising at least one] defined by a plurality of laser machined grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated from one another by remaining portions of the conductive layer;

[each conductor configured for electrical communication with a semiconductor die;]

at least one semiconductor die on the first surface in electrical communication with the conductors;

a plurality of conductive vias in the substrate in electrical communication with the conductors; and

a plurality of external contacts on the second surface in electrical communication with the conductive vias.

26. (amended) The semiconductor component of claim 25 further comprising a plurality of bond pads on the conductors and the semiconductor die is wire bonded to the bond pads.

[a plurality of semiconductor dice wire bonded to the conductors.]

27. (amended) The semiconductor component of claim 25 further comprising a plurality of bond pads on the conductors and the semiconductor die is flip chip mounted to the bond pads.
[conductors.]

28. (amended) The semiconductor component of claim 25 wherein the substrate comprises a material selected from the [class] group consisting of plastic, glass filled resin, silicon and ceramic.

29. (amended) The semiconductor component of claim 25 wherein the external contacts comprise balls in a [ball] grid array.

30. (amended) A semiconductor component comprising;

a substrate comprising a surface;

[with]

a conductive layer [thereon] on the surface having a thickness;

[and]

a plurality of conductors on the surface [, the conductors comprising] defined by a plurality of pairs of laser machined grooves through the thickness of the conductive layer, each conductor comprising a portion of the conductive layer which is electrically isolated on either side by a pair of laser machined grooves; and

a semiconductor die on the surface in electrical communication with the conductors.

[the conductors including a first conductor configured as a signal path for the component and a second conductor in electrical communication with a ground or voltage path, with the thickness of the conductive layer and a width of the grooves selected to provide an impedance value for the first conductor.]

31. (amended) The semiconductor component of claim 30 further comprising a laser machined opening in the conductive layer configured for mounting the semiconductor die to the substrate.
[plurality of external contacts on the substrate in electrical communication with the conductors.]

32. (amended) The semiconductor component of claim [31] 30 further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors and with a plurality of [external] contacts [formed] on a second surface of the substrate.

33. (amended) The semiconductor component of claim [32] 30 wherein the semiconductor die is flip chip mounted or wire bonded to the conductors.
[further comprising a semiconductor die mounted to the substrate in electrical communication with the conductors.]

34. (amended) The semiconductor component of claim [33] 30 further comprising an [encapuslant] encapsulant covering the semiconductor die and at least a portion of the surface.

35. (amended) A semiconductor component comprising:
a substrate comprising a surface;
[with]
a conductive layer [thereon, the conductive layer] on the surface having a thickness;
a plurality of [laser machined] conductors on the surface comprising portions of [in] the conductive layer, each conductor defined and electrically isolated by a pair of laser machined grooves through the conductive layer; and
[, the conductors including a plurality of first pads;]

a semiconductor die [mounted to] on the substrate in electrical communication with the conductors;

[, the die comprising a plurality second pads bonded to the first pads; and]

with the thickness of the conductive layer, and a width of the [grooves] conductors selected to provide [an] a selected impedance for the conductors.

36. (amended) The semiconductor component of claim 35 further comprising an encapsulant covering the semiconductor die and at least a portion of the surface.

37. (amended) The semiconductor component of claim 35 further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors and with a plurality of [contact balls formed] external contacts on a second surface of the substrate.

38. (amended) The semiconductor component of claim 35 wherein the substrate comprises silicon [with] and an electrically insulating layer on the surface.

39. (amended) The semiconductor component of claim 35 wherein the substrate comprises a material selected from the [class] group consisting of plastic, glass filled resin and ceramic.